UPF Analyzer

The Front-End for Power Aware EDA Tools

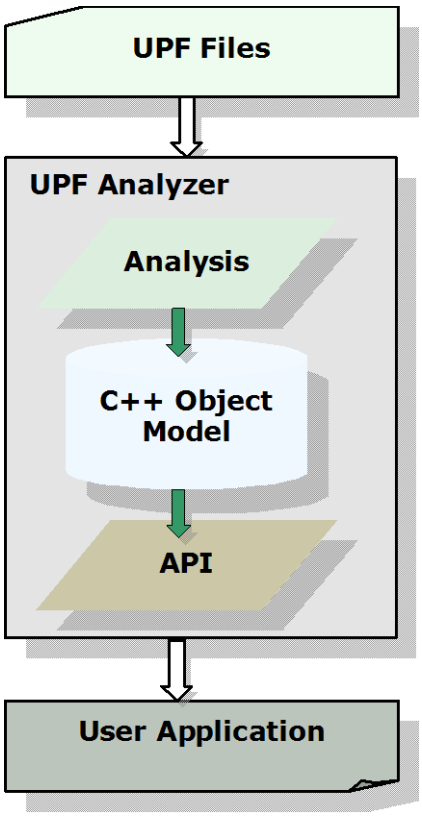
Highlights

- A customizable framework for annotating power intent into the design at any stage in the design flow: RTL, logic, placement
- Support for all UPF commands as in Version IEEE-1801
- Flexible and easy to integrate C++ interface
- Dynamic and extensible Object Model
- Internal memory manager for optimum use of memory
- Customizable error callback routines that return file name and line numbers
- Can be easily integrated with existing tools built on top of TCL interpreter
- Fully re-entrant flow
- Is backed by Interra's field-proven expertise in developing analyzer and synthesis libraries

Addressing the needs of EDA tool developers who need a syntax checker plug-in for IEEE Unified Power Format (UPF), now standardized by IEEE, Interra offers UPF Analyzer – A TCL based syntax and semantic validator for UPF. Available as an efficient and customizable plug-in, the UPF Analyzer assures faster time-to-market for UPF-based tools in the low power domain.

UPF Analyzer performs complete syntax check for all the UPF commands in accordance with UPF Version IEEE 1801-2009 (UPF 2.0). In addition, the analyzer performs implicit semantic validation for the UPF commands. The UPF analyzer uses an efficient C++ object model to represent the contents of a UPF file. The object model can be easily accessed using the analyzer's C++ interface enabling seamless integration with C++ based EDA Tools.

UPF Analyzer is available on Solaris, Linux, and Windows platforms.



The UPF Analyzer Features

Complete Support for IEEE 1801-2009 (UPF 2.0)

The analyzer performs syntax and semantic validation for all the commands in accordance with IEEE 1801-2009 (UPF 2.0). However we continue to support UPF Version 1.0, February 22, 2007.

Extension of TCL Library

The UPF analyzer is an extension of the TCL interpreter and supports all the in-built TCL commands.

The analyzer uses TCL8.4 library. The TCL library has been customized to get the line number and file name.

C++ Class Hierarchy Accessed Through C++ Interfaces

The analyzer provides an efficient and robust C++ class hierarchy for storing the power information. This information can be easily accessed through the C++ interface of the analyzer.

Editable Object Model

The analyzer's object model is dynamic and editable. C++ based applications can access the object model using the analyzer's C++ interfaces. This gives the extra power to those EDA tools that read UPF power information as input and then writes out a different UPF by taking care of name mapping from RTL to gate-level netlist. The analyzer also provides a framework to create the UPF object model from scratch!

Reuse of Customized TCL Interpreter

User applications, which have a customized TCL interpreter for reading other TCL based formats, such as SDC (Synopsys Design Constraint), can simply re-use the already customized TCL interpreter and extend it by adding UPF related commands into it.

Configurable Error Callback

The analyzer allows registration of custom error messages for application-specific needs.

Flat and Hierarchical Views

Netlist hierarchies are available in both flat as well as hierarchical view.

Based on user-defined options, all the network elements, such as ports, nets, power switches, and domains get promoted to the same level while maintaining respective connections. The flat netlist can also be converted back to a hierarchical format. Flat and hierarchical scopes can also be dumped in separate files.

Efficient Power State Table Processing

If more than one Power State Table (PST) is specified within a scope then they can be merged into one. The merged PST does not contain any duplicate or inconsistent states w.r.t. connected supplies. Similarly, while creating hierarchies from flat netlist, the analyzer can split the PST with relevant supplies for the scope being created.

Also available:

- Cheetah System Verilog Analyzer
- Jaguar VHDL Analyzer
- Analyzers for CPF, HSPICEE, SDF, SPF (DSPF/RSPF), SPEF, LEF, DEF, SAIF, and VCD.

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