MC2

Accelerating Memory Design

Traditional tools are unable to meet the needs of today's memory designers. Designs of standard memory products are rarely reused and have to be manually recreated for every new design. Addressing these limitations, Interra's MC2 provides a complete memory development system that enhances a designer's productivity and reduces design iterations.

MC2, an automated and proven memory development system, targets embedded and discrete memories. MC2 automates the overall methodology for the design and distribution of memories, helping designers create solutions more rapidly. Empowering memory designers to design new memory instances, leverage existing designs, target new processes, create new memory architectures, MC2 increases productivity and promotes the reuse of design IPs. MC2 offers unique scalability for density as well as seamless migration to new sub-micron processes. Customers using MC2 are expected to save over 40% of their development resources and time in the first project alone. Incremental savings can be expected over time. In addition, MC2 generates reusable memory architecture for secure distribution to ASIC & SoC designers.
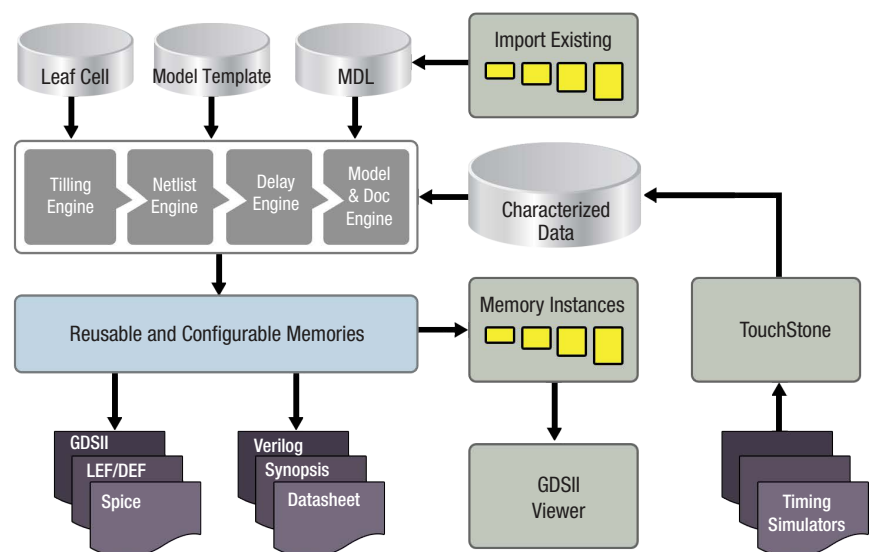
MC2 is available on Linux platform.

Advantages

- **Improved Productivity**
  Automates memory design and reduces design iterations and manual effort in memory development

- **Rapid Scalability**
  Increased densities of similar designs can be quickly created

- **Process Transparency**
  The same set of input files can be reused for low power, ultra low power, and high voltage designs for the same process technology

- **Reuse of IP Assets**
  Enables reuse of a core design and development of newer products easily

- **Ease of SoC Design**
  Automates memory designing in SoC or ASIC

- **TRC (Tiling Rules Checker)**
  Detects potential DRC/LVS errors at an early stage

- **Easily Integrated into the Design Flows**
  Can be modified for user-specific requirements

- **Field-proven Quality**
  Tested processes offer predictable quality

Highlights

- Automatic Tiling and Netlisting
- Verilog and Spice Netlist for LVS
- Full Physical Views – GDSII & LEF
- Automatic generation of Timing Model and Data Sheet
- Ability to import existing memories
- Capable of programming ROMS
- Ability to create GDS and Spice Donut
- Memory Characterization Framework
- Fully integrated Layout Viewer and Tiling Debugger

TouchStone: Memory Characterization platform from Interra Systems.

MDL - Memory Description Language

MC2 provides a programming interface through MDL, a proprietary language from Interra. MDL is a Perl-like programming language and is robust and easy to learn. MDL enables memory designers to describe the placement of leaf cells. MDL supports various functions, such as rotation, mirroring, arraying along x/y axis, pattern repetition, partial patterns and nested patterns.

Tiling Engine

Increasing a memory designer's productivity when creating multiple configurations, the Tiling Engine automates leaf cell placement, power ring/mesh generation, pin routing, and outputs GDSII and LEF views for each memory core. Tiling engine supports creation of Donut GDS.

Netlist Engine

MC2 supports hierarchical and at design methodologies within the netlist engine. You can design hierarchically, creating small building blocks and reference them into larger building blocks. MC2 automatically creates Netlist from physical connections and supports industry standard SPICE and Verilog data formats for functional verification and LVS.

Power Ring/Mesh Generation and Pin Routing

MC2 automates the generation of power ring/mesh and pin routing. You can specify the spacing between inner/outer power rings and metal layers, decide metal widths, route non-boundary pins, overlay pin boxes, and use MDL functions to apply design rules.

Internal Routing and Power Bridging

MC2's support for routing includes: Internal Routing, which enables you to generate internal routes between data pins that have the same name; and, Power Bridging, which enables you to bridge power pins that are separated because of gaps between two cells. MC2 handles non-aligned pins and imperfect bridging scenarios.

ROM Personalization

MC2 enables you to program ROM contents by specifying logical to physical mapping of the ROM content in GDSII form. MC2 supports both linear and non-linear program scrambling.

Delay and Power Module

MC2's Delay and Power feature, which implements a programmable delay calculator, can be tailored to user-specific characterization methodology. You can also specify the delay and power equations and de-rating factors.

Module and Document Generation

MC2's flexible timing model and data sheet generation enables designers to support timing models, for any mix of tools from different EDA vendors, by providing templates for them. Data sheets can also be generated in HTML/XML format. MC2's reusable memory architecture enables end-users to quickly update model generators for new EDA tool revisions resulting in reduced turn-around time.

MDL Code Coverage Analyzer

MC2's MDL Code Coverage Analyzer automates the testing of MDL code. The MDL Code Coverage Analyzer generates a list of memory configurations that covers all corner cases in an MDL placement le. QA and verification cycles can then be run on these configurations.

Tiling Rule Checker

MC2's Tiling Rule Checker detects memory tiling issues, such as misaligned geometries, unmatched geometries, improper rotation/mirroring that may cause improper power connections at the memory architecture development stage. Tiling Rule Checker ensures that the memory has less number of potential errors when the memory architecture is generated. Thus, potential DRC errors are fixed at an early stage in memory development.

GDS Viewer and GDS Import

GDS Viewer lets you view the generated GDSII at various level of granularity. Integrated with the Graphical User Interface, the GDS Viewer provides a single framework for the memory designer to tile and view the memory without having to use a layout editor. Designs can be imported into MC2 framework using the GDS import feature. This feature automatically generates MDL from GDSII of pre existing designs.

Secure Distribution

MC2 automatically creates secure, encrypted package of the memory architecture for distribution to memory users. The encrypted package generates memory instances from the encrypted file without recreating any original files on disk.

interra systems