Beacon-2k1

interra systems

Comprehensive Test Suite for Verilog-2001 & 2005 Compliance

Key Advantages

- Field-proven test suite that has been used to mature several industry-standard EDA tools
- Developed in partnership with significant EDA majors
- Conforming to accepted definition and interpretation of the language
- Providing an unbiased quality analysis of EDA tools
- Complete coverage of constructs and styles
- Comprehensive validation of syntax, synthesizability, and simulation semantics

Highlights

- Over 5,000 test cases along with test benches
- Golden output for comparison
- Detailed test plans with cross-reference to test cases
- Well organized test cases highlighting testing objectives
- Both positive and negative test cases

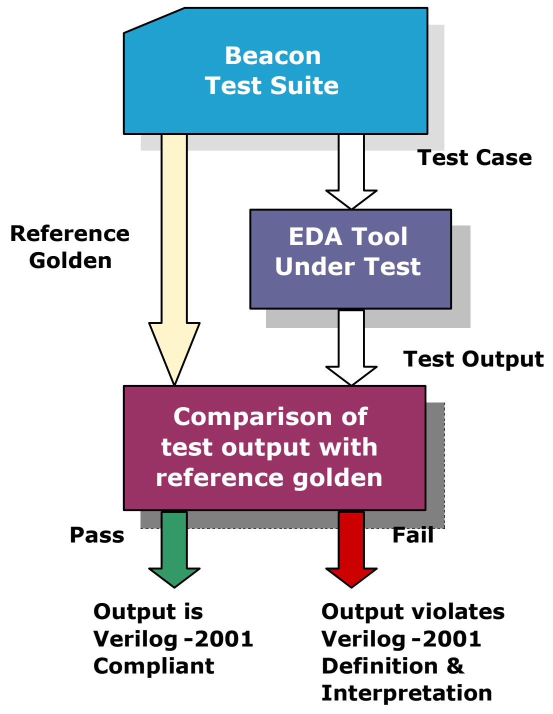
Addressing the needs of EDA tool developers to quickly evaluate the quality of their products, Interra's Beacon-2k1 delivers a comprehensive test suite based on Verilog-2001 and 2005 (IEEE-1364-2001 and IEEE-1364-2005) standards.

You can use Beacon-2k1 to characterize EDA tools for coverage and quality across various language constructs and styles.

Enabling you to discover language and RTL non-compliance early in the product development and testing life cycle, Beacon-2k1 offers:

- Reduced development costs and time-to-market EDA products
- Development of standard-based products
- Precise evaluation of bugs and errors in the product
- Measure of product quality
- Unbiased feedback on product quality
- Regression tests for quality assurance

The test cases and test benches can be applied to the EDA tool under evaluation and results can be compared with golden reference that is provided with Beacon-2k1.


Beacon Test Suite
Test Case
Reference Golden
EDA Tool Under Test
Test Output
Comparison of test output with reference golden
Pass
Fail
Output is Verilog -2001 Compliant
Output violates Verilog -2001 Definition & Interpretation

The Beacon -2k1 Features

Comprehensive Test Suite

Covers various new Verilog -2001 and 2005 constructs and styles. The test cases enable you to evaluate syntax, semantics, synthesizability, and simulation aspects of a Verilog -2001 & 2005 -based tool.

Syntax and Semantics Cover

Beacon -2k1 includes over 5,000 test cases that cover Verilog constructs and styles as specified in the table below. Along with positive test cases, there are negative test cases that validate correct behavior by taking in erroneous inputs.

Language Construct	Number of Test Cases
ANSI Style Ports	73
Auto Width Extension	16
Multi Dimension Arrays	446
Continuous Assignments without Net Declarations	30
Attributes	537
Event Control	32
Combination of Constructs	1,773
Configuration	221
Constant Functions	65
Combined port/data	118
Disable Default Net	8
Compiler Directives	15
Command Parsing	14
SDF File Support	3
VCD Enhancement	18
File IO	50
Generate Statement	367
Instance Array	30
Negative Pulse Detection	37
Arithmetic Operators	53
PLA Modeling	25
Parameters	492
Indexed Part Select	442
Pulse Error Propagation	20
Signed Arithmetic	53
Reentrant Task/Functions	28
Timing Checks	44
Variable Declaration Assignments	62
Verilog 2005	208
Total	**5,266**

Synthesis Subset Cover

Exhaustive test cases cover supported and unsupported styles and constructs for synthesis under a combination of constructs category.

Simulation Cover

Positive test cases, with test benches and expected output, validate simulator and equivalent tools.

Well Documented Test Plans

The test plans describe all test objectives and are categorized by sections. Each test case has a reference to the section number of the test plan.

Test Benches and Reference Golden

Provides test benches to instantiate test cases and apply vectors on inputs. Outputs are captured after an appropriate interval and written on to a file. Reference golden output is also provided for these test benches for all the test cases. You can easily apply the test bench to the test tool and compare the outputs.

Sample Test Case

```
--** Purpose:        Net array declaration with vector
                     data. Reading correctly through
                     parameter
--** LRM :           Sections 3.10
--** TestPlan:       Sections 5.1.4.5
--** Kind :          Simulation
--** Status:         SIMULATION_SHOULD_PASS

*********************************

`timescale 1ns/1ns

module top(data, in);
    wire [3:0]netArray[3:0][4:0];
    output [3:0]data;
    input [3:0] in;
    parameter p2=3;
      assign netArray[3][2][p2] = ~in;
      assign data[1] = netArray[3][2][p2];
endmodule
```

Interra Systems, Inc.
1601 S. De Anza Boulevard, Suite 212, Cupertino, CA 95014
Phone : +1 408 579 2000, Fax: +1 408 579 2050
Email: info@interradesign.com Web: www.interradesign.com